

A Self-Clocked ASIC Interface for MEMS Gyroscope with $1\text{m}^\circ/\text{s}/\sqrt{\text{Hz}}$ Noise Floor

A. Elsayed, A. Elshennawy, A. Elmallah, A. Shaban,
B. George, M. Elmala, A. Ismail, A. Wassal, M. Sakr,
A. Mokhtar, M. Hafez, A. Hamed, M. Saeed,
M. Samir, M. Hammad, M. Elkhouly, A. Kamal
ASIC Solutions Division
Si-Ware Systems
Cairo, Egypt

M. Rabieah, A. Elghufaili,
S. Shaibani, I. Hakami, T. Alanazi
Electronics, Communications & Photonics Program
King Abdulaziz City for Science and Technology (KACST)
Riyadh, Saudi Arabia

Abstract—An interface for MEMS gyroscope is implemented in $0.18\mu\text{m}$ HVC MOS technology, and achieves a low noise floor of $1\text{m}^\circ/\text{sec}/\sqrt{\text{Hz}}$ over 200Hz BW. Electromechanical $\Sigma\Delta$ force-feedback and self-clocking scheme based on gyro resonance are implemented. The interface includes on-chip reference generation, decimation, and temperature compensation.

Keywords—gyroscopes; Sigma delta modulation; Force feedback; Self-clocking; MEMS; Coriolis force

I. INTRODUCTION

The market growth of micro-machined gyroscope applications is pushing for developing high performance interface solutions. Electrostatic force feed-back reduces sensitivity to process variations affecting the gyro, increases BW and linearity, and allows operation in matched mode [1]. This paper presents a fully integrated ASIC to interface with MEMS gyroscopes in closed loop configuration for best performance in harsh environment. Incorporating the gyro as a part of the force-feedback loop filter converts the system to a hybrid electromechanical $\Sigma\Delta$ modulator with a continuous time (CT) part represented by the mechanical filter and a discrete time (DT) part represented by the electronics filter.

The paper starts with a brief description of the self-clocking scheme benefits. Then, section III, gives an overview on the solution architecture, highlighting the main components. Section IV, shows the implementation details, and lists some key measurements results. Section V, concludes the paper.

II. SELF-CLOCKING

The CT nature of the mechanical filter makes the performance of the $\Sigma\Delta$ modulator sensitive to the exact feedback pulse shape. For this reason, low-jitter clock is required for best performance with force feed-back. The chip includes a PLL that uses a reference clock generated using the high quality (Q) resonance of the gyro oscillation. This arrangement results in a self-clocked system that does not need an external crystal, and leads to a low noise floor at the system output. Moreover, using a gyro based reference clock allows fixing the ratio between the system sampling frequency and the

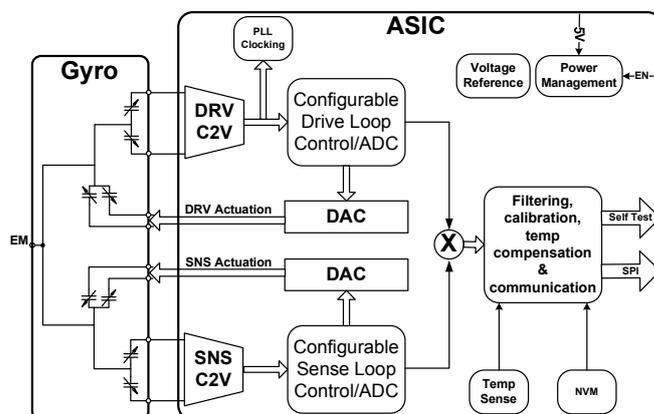


Figure 1. ASIC/Gyro system architecture.

mechanical drive resonance frequency (Coriolis signal carrier). Therefore, this scheme enables interfacing to a wide-range of gyro modules.

III. ARCHITECTURE

Fig. 1 shows the block diagram of the ASIC interfaced to a MEMS gyro. The system is composed of a programmable low noise capacitive sensing front end, high resolution ADC for capacitive digitization, and digital processing, forming the drive and sense loops. Also, the ASIC has a standard SPI interface. The ASIC is powered from a single 5V supply and uses an integrated voltage charge pump for improved start-up time. The chip includes on-chip temperature sensing and compensation, and employs a low-noise band-gap reference (BGR) core that generates a 1.2V reference voltage needed by power-management regulators and other bias cores. In addition, the BGR circuit supplies a buffered version of the reference voltage to each ADC of the drive and sense loops, in addition to the excitation/actuation switches and the temperature sensor.

A. Drive Loop

The drive loop, shown in Fig. 2(a), incorporates the phase shift required to achieve the oscillation condition as well as an automatic gain control loop (AGC) to control the amplitude of oscillation of the mechanical element. A 4th order band pass $\Delta\Sigma$ modulator, composed of two resonators with feed forward coefficients, converts the drive loop C/V output into single bit reading of the gyro drive oscillation signal. In order to obtain drive startup time less than 1s, it is necessary to maximize actuation voltage value. An internal voltage charge pump generates 10V reference during gyro startup and is disabled

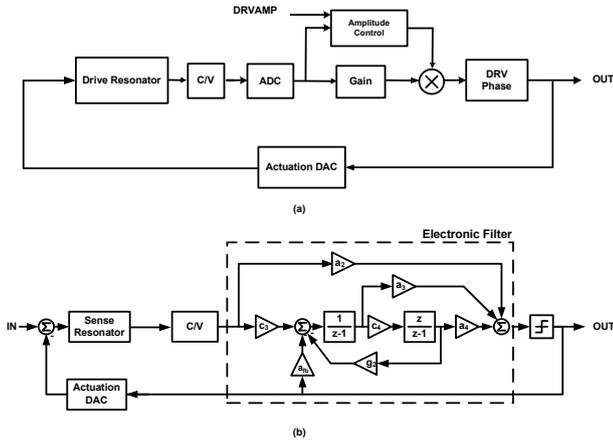


Figure 2. (a) Drive loop implementation. (b) Sense loop implementation.

during normal operation. The gyro drive actuation switches are LDMOS type to avoid reliability issues.

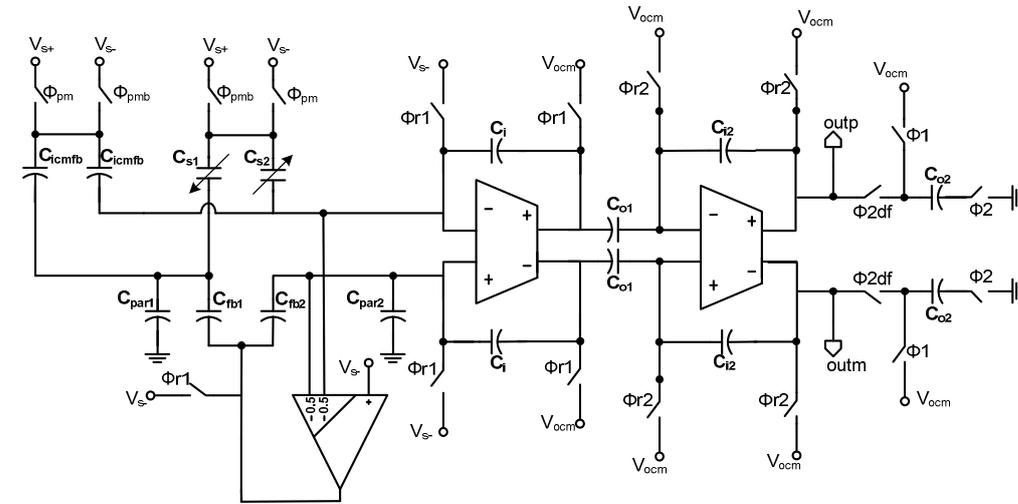
B. Sense Loop

The sense loop, shown in Fig. 2(b), performs force feedback control on the gyro MEMS capacitive sense electrodes, and provides a digital output reading. The low-jitter clocking of the self-clocked ASIC achieves better SNR for CT force-feedback operation. The loop is achieved by implementing a 4th order electro-mechanical $\Delta\Sigma$ modulator using a switch-cap electronic filter. The modulator architecture is based on feed-forward topology with a feed-back branch to stabilize the loop [2].

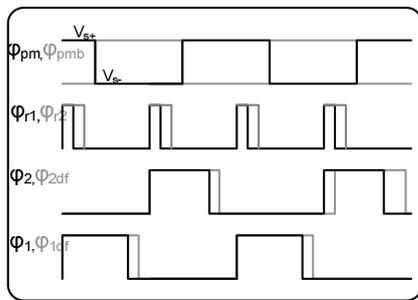
C. Capacitance to Voltage Front End (C/V) Interface

The capacitance-to-voltage front end (C/V) interface, shown in Fig. 3, is implemented using a switched capacitor amplifier. The excitation signal is applied as a square wave common-mode signal on the Proof Mass (PM) of the mechanical element. This allows the separation of the drive and sense signals (and possibly additional axis, if exists) physically on different capacitors. An input common-mode feedback loop is implemented to remove the common-mode component resulting from the common-mode excitation [3].

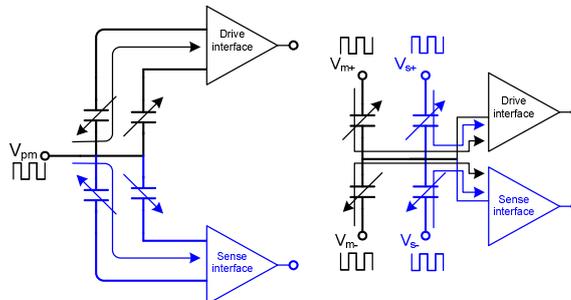
Two Programmable Capacitor Arrays (PCA) are added and excited with an opposite excitation signal. These PCA are used to remove the offset of the differential MEMS capacitors and to help in removing the common-mode step caused by the PM



(a) Schematic of C/V circuit.



(b) Clock signals.



(c) Excitation at the proof mass.

(d) Excitation at the end terminals.

Figure 3. C/V circuit and timing diagram.

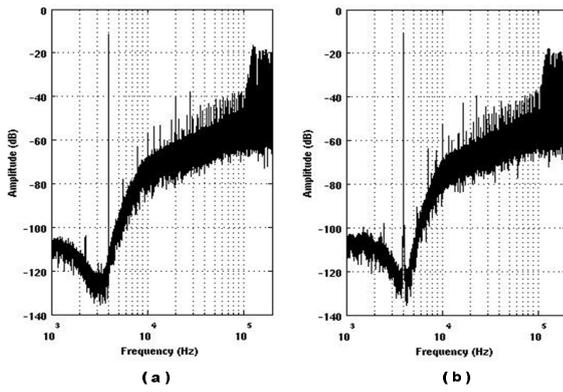


Figure 4. Drive loop output spectrum (a) without self-clocking (b) with self-clocking.

signal. The second stage employs Correlated Double Sampling (CDS) technique to remove the low frequency noise and offset of both first and second stages. The drive mode C/V is followed by a sample and hold, a CT filter, and a differential-to-CMOS converter to generate the reference signal of the PLL to enable the ASIC self-clocking. The same architecture of the C/V is used in both drive and sense modes with different C/V gain.

D. DSP Core

The DSP core filters the output of the $\Delta\Sigma$ modulators of both the drive and sense loops, implements a digital drive loop

using the output of the drive $\Delta\Sigma$ modulator, and performs the final output demodulation. The demodulation output is decimated using a programmable decimation filter. Two BPF's centered at the gyro resonance frequency with 200Hz BW, filter out noise of both the drive and sense output signals, before multiplying them for demodulation. Hence, mixing and down conversion of quantization noise to the band of interest are avoided. The poles and zeros of each BPF scale with the sampling frequency (depending on the gyro module), and therefore the center frequency will be correctly tuned with variations of the gyro resonance frequency. Accurate adjustment of the phase shift is necessary to suppress the quadrature signal and provide maximum signal gain. The DSP system adjusts this phase shift for proper demodulation. The digital output interface allows seamless integration of the ASIC compared to analog output interfaces [4].

The DSP core supports run-time self-test functionality to assure fail-safe operation. This is done by monitoring the status of the main sub-systems; where a flag represents the proper functionality mode of each one. The length of the bit-stream run count is used to indicate a stable sense loop. The drive loop amplitude of oscillation is monitored to be between upper and lower limits. A lock detector is used to indicate the locking of the PLL.

E. Temperature Sensing

The temperature sensing system measures the die temperature and converts it into a digital reading, which is used for temperature compensation of the scale factor and the zero-

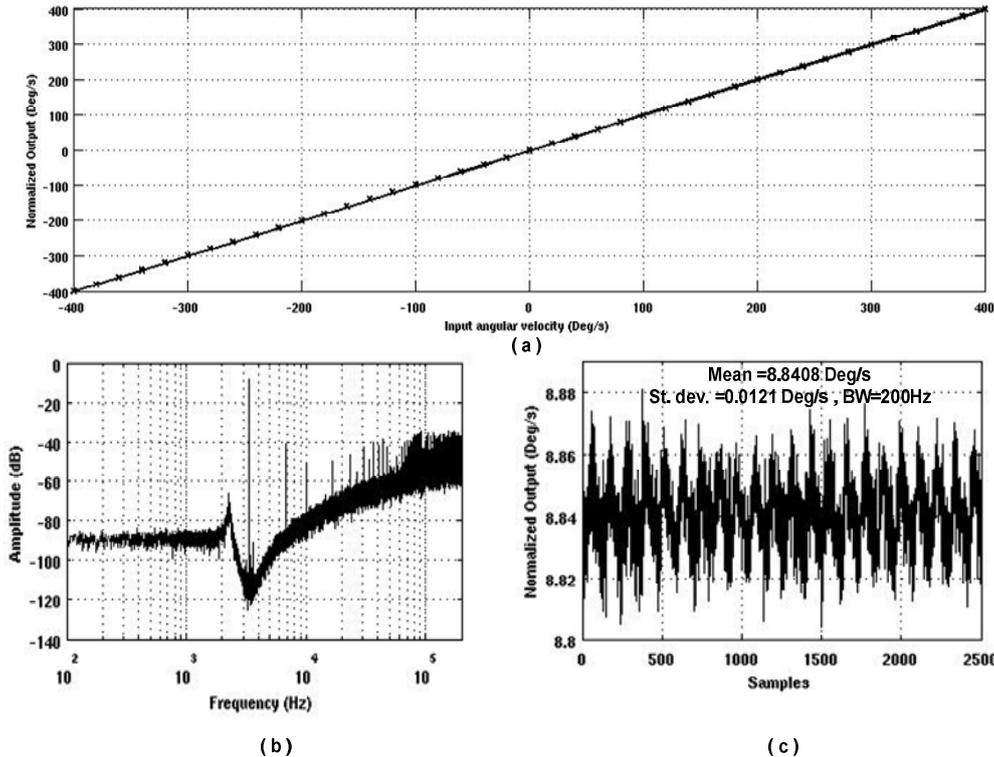


Figure 5. (a) DC transfer function (normalized output digital reading against input angular velocity) (b) Output spectrum of the sense loop (c) Interface output reading, indicating ZRO of $9^\circ/\text{s}$ and noise floor of $860\mu^\circ/\text{s}/\sqrt{\text{Hz}}$.

rate output (ZRO) of the gyro reading. Temperature sensing is performed via a PTAT sensor. A first order incremental $\Delta\Sigma$ ADC, consisting of a switched capacitor integrator and a comparator, digitizes the sensor's output providing a digital representation of the temperature. The switched capacitor integrator provides the required scaling and shifting of the sensor's output to be centered within the dynamic range of the ADC.

IV. IMPLEMENTATION AND MEASUREMENTS

The ASIC is fabricated in 0.18 μm HVCMOS technology featured with 10V LDMOS devices. The chip area is 28mm². The power supply used is 5V and the total power consumption is 320mW, including power management and digital sections. The ASIC and gyroscope are combined in a single LCC package.

The drive loop spectrum with and without self-clocking option is shown in Fig. 4. The self-clocking enables centering the drive signal in the pass-band of the $\Sigma\Delta$ modulator. The DC transfer function of the sensor is shown in Fig. 5(a). The maximum input range is $\pm 400^\circ/\text{s}$ and is limited by the rotating table range. The ASIC achieved DC linearity of 0.26% of the full-scale input. The output spectrum of the sense loop is shown in Fig. 5(b). The interface output reading is shown in Fig. 5(c), indicating in-band spot noise floor of $860\mu^\circ/\text{s}/\sqrt{\text{Hz}}$, which is lower than reported spot noise floor values in literature [1-4]. The system parameters and measured performance are summarized in Table. 1. Fig. 6, shows the ASIC die, and the ASIC/Gyro packaging photograph.

V. CONCLUSION

This paper describes an ASIC interface for MEMS gyroscopes. The ASIC employs electromechanical force feedback sensing loop which provides stable operation in harsh environments, and allows benefiting from matched mode operation without compromising the signal bandwidth. Self-clocking scheme is implemented which allows using the high quality MEMS resonator to function as a clean reference to the main system clock. The low jitter performance of the

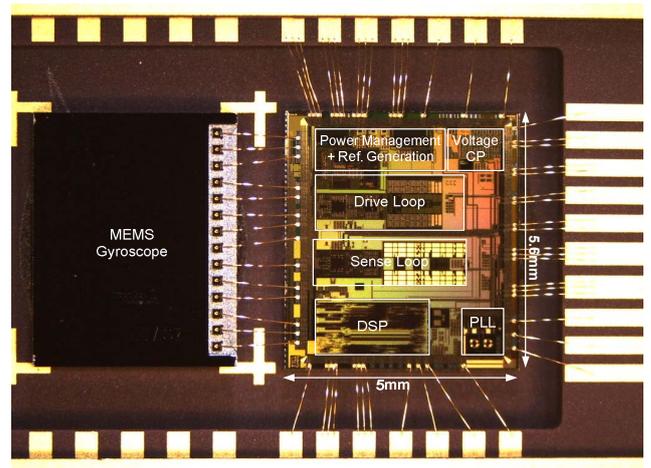


Figure 6. ASIC/Gyro packaging photograph.

self-clocking scheme is mandatory for the CT feedback of the sense loop. The self-clocking scheme also permits an automatic synchronization of the zeros of the BP- $\Sigma\Delta$ modulators used in both sense and drive loops. This scheme helps achieving superior noise performance with floor lower than $1\text{m}^\circ/\text{s}/\sqrt{\text{Hz}}$.

The ASIC provides a fully integrated solution with on-chip reference generation, power management, temperature sensing, and clock generation. In addition to a complete DSP solution for signal processing including decimation filters, ZRO cancellation, temperature compensation of both the scale factor and ZRO, and a standard serial interface channel. The DSP also generates a self-test signal that allows a fail-safe operation

The ASIC is fabricated in 0.18 μm HVCMOS process, occupies 28mm², and dissipates 320mW from a single 5V supply. The ASIC is packaged along with the MEMS gyroscope in a single LCC packaging solution.

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TABLE I. SYSTEM PARAMETERS AND MEASURED PERFORMANCE.

Process technology	0.18 μm 2P6M HVCMOS
Chip area (mm ²)	28 (5mmX5.6mm)
Packaging	LCC36 (MEMS + ASIC)
Supply voltage (V)	5
Chip supply current (mA) (Including: power management + reference generation + decimation filter)	64
Sensitivity to linear motion ($^\circ/\text{s}/\text{g}$) (Acceleration from 20Hz to 2kHz)	0.1
Full scale signal (Limited by rotating table range)	± 400
Noise Floor ($^\circ/\text{s}/\sqrt{\text{Hz}}$)	1m
DC Linearity (%Full scale)	0.26
BW (Hz)	200
Startup time (s)	0.5